PATENT APPLICATION

for

TRANSMISSION LINE PARASITIC ELEMENT DISCONTINUITY CANCELLATION

by

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Attorney Docket No. 20206-027 (P00-2898)

TRANSMISSION LINE PARASITIC ELEMENT DISCONTINUITY CANCELLATION

CLAIM OF PRIORITY

The present application claims the benefit of and incorporates by reference U.S. Provisional Application Serial No. 60/239,020, filed October 4, 2000.

FIELD OF THE INVENTION

The present invention generally relates to the transmission of signals within an electronic device and, more particularly, to a system and method for enhancing the integrity of transmitted signals within an electronic device by canceling the effects of parasitic capacitance in the medium used to transmit signals.

BACKGROUND OF THE INVENTION

Buses are commonly used in computers and other electronic devices to send signals containing data from a driving (or generation) point to any number of receiving points. These busses can be created in printed circuit technology or from cables attached from one point to a second point. Backplane buses use circuit cards that plug in at regular intervals and represent loads along the bus. Cable busses employ cables with uniform electrical parameters that are connected at load devices in, for example, a daisy-chain fashion. Such a connection is used, for example, in Small Computers Systems Interface (SCSI) implementations.

The SCSI type of bus is also adaptable for use within backplane architectures. In systems of this type, the cable bus is replaced with a printed circuit board backplane. Intelligent peripheral devices, in the form of daughter boards, are then connected to the backplane connectors. The backplane architecture provides a compact and efficient method for connecting a series of intelligent peripheral devices to a computer system.

To work properly, a bus must maintain certain electrical characteristics. One of these characteristics is a controlled impedance. For an unloaded bus (i.e., a bus with no attached intelligent peripheral devices), the intrinsic impedance (Z.sub.0) can be calculated using the intrinsic impedance per unit length (L.sub.0) and the intrinsic capacitance per unit length (C.sub.0) in the following equation:

Z.sub.0 =(L.sub.0 /C.sub.0).sup.1/2

For a loaded bus, the preceding equation must be modified to reflect the effect of the attached load devices. This is most always in the form of added capacitance attributable to the attached load devices. Specifically, for a loaded bus the impedance (Z') can be calculated by modifying the preceding equation to include the load capacitance per unit length (C.sub.d) resulting in the following equation:

Z'=(L.sub.0 /(C.sub.0 +C.sub.d)).sup.1/2